

HLDVT '03

Eighth Annual IEEE International Workshop on High Level Design Validation and Test

November 12-14, 2003
Hyatt Regency Hotel, San Francisco, California

WED, NOV 12

5:00-7:30pm Registration

7:30-9:30pm Buffet Reception

THUR, NOV 13

7:00-8:00am Continental Breakfast

8:15-8:30am Welcome Remarks

Session 1 8:30-10:15am *Invited Special Session: Nano, Quantum and Molecular Computing: Challenges in Verification and Test*

Organizers: Sandeep Shukla, Virginia Tech; Ramesh Karri, Polytechnic Univ.
Speakers to include: Sankar Basu, Natl. Science Foundation; Kaustav Banerjee, Forrest Brewer, University of California, Santa Barbara

10:15-10:45am Break

Session 2 10:45-12:00pm *Processor Validation and Test*

Software-Based Self-Test Methodology for Crosstalk Faults in Processors
Speakers to include: Xiaoliang Bai, Li Chen, Sujit Dey, University of California, San Diego

FPgen - A Test Generation Framework for Datapath Floating-Point Verification
Speakers to include: Merav Aharoni, Sigal Asaf, Laurent Fournier, Anatoly Koifman, Raviv Nagel, IBM

Piparazzi: A Test Program Generator for Micro-architecture Flow Verification
Speakers to include: Allon Adir, Eyal Bin, Avi Ziv, IBM Research Lab at Haifa

12:00-1:15pm Lunch

Session 3 1:15-2:30pm *High-Level Design Transformations*

Automatic Functional Verification of Memory Oriented Global Source Code Transformations
Speakers to include: K.C. Shashidhar, Maurice Bruynooghe, Francky Catthoor, Gerda Janssens, Katholieke Universiteit Leuven, Belgium

Refactoring Digital Hardware Designs with Assertion Libraries
Speakers to include: Claudionor Coelho, Jose Nacif, Antonio Fernandes, Diogenes da Silva, Universidade Federal de Minas Gerais, Brazil; Harry Foster, Jasper Design Automation; Flavio de Paula, Joseph Tompkins, Mindspeed Technologies, Inc.

High-level Optimization of Pipeline Design
Speakers to include: Jennifer P.L. Campbell, Nancy A. Day, University of Waterloo

2:00-3:00pm Break

Session 4 3:00-4:15pm *SAT and Applications*

Integrating CNF and BDD Based SAT Solvers
Speakers to include: Sivaram Gopalakrishnan, Vijay Durairaj, Priyank Kalla, University of Utah

Logic Transformation based approach to SAT Solver
Speaker: Dhiraj Pradhan, University of Bristol

Enhancing SAT-based Equivalence Checking with Static Logic Implications
Speakers to include: Rajat Arora, Michael S. Hsiao, Virginia Tech

4:15-4:45pm Break

Session 5 4:45-6:00pm *System-Level Issues*

Relating vehicle-level and network-level reliability through high-level fault injection
Speakers to include: Fulvio Corno, Paolo Gabrielli, Simonluca Tosato, Politecnico di Torino

Testing ThumbPod: Softcore Bugs are Hard to Find
Speakers to include: Patrick Schaumont, Kazuo Sakiyama, Yi Fan, David Hwang, Shenglin Yang, Alireza Hodjat, Bocheng Lai, Ingrid Verbauwhede, UCLA

Verifying LOC Based Functional and Performance Constraints
Speakers to include: Xi Chen, Harry Hsieh, University of California, Riverside; Felice Balarin, Yosinori Watanabe, Cadence Berkeley Laboratories

FRI, NOV 14

7:00-8:00am Continental Breakfast

Session 6 8:00-9:40am *Functional Vector Generation and Coverage*

Comparison of Bayesian Networks and Data Mining for Coverage Directed Verification
Speakers to include: Markus Braun, Wolfgang Rosenstiel, Klaus-Dieter Schubert, Tübingen University

Enhancing the Control and Efficiency of the Covering Process
Speakers to include: Shai Fine and Avi Ziv, IBM Research Lab at Haifa

Functional Vector Generation for Assertion-Based Verification at Behavioral Level Using Interval Analysis
Speakers to include: I. Ugarte, P. Sanchez, University of Cantabria

Redundant Functional Faults Reduction by Saboteurs Synthesis
Speakers to include: Franco Fummi, Cristina Marconcini, Graziano Pravadelli, Università di Verona

Detailed information can be found on the
HLDVT web site

<http://www.hldvt.com/03/>

9:40-10:10am Break

Session 7 10:10-11:50am *Advances in Sequential Verification*

ATPG-based PreImage Computation: Efficient Search Space Pruning With ZBDD
Speakers to include: Kameshwar Chandrasekar, Michael S. Hsiao, Virginia Tech

BDD-Based Verification of Scalable Designs
Speakers to include: Daniel Große and Rolf Drechsler, University of Bremen

Matching in the presence of don't cares and redundant sequential elements for sequential equivalence checking
Speakers to include: Solaiman Rahim, Synplicity-LIRMM, France; Bruno Rouzeyre, Lionel Torres, LIRMM, France; Jerome Rampon, Synplicity, France

Mathematical Framework for Representing Discrete Functions as Word-level Polynomials
Speakers to include: Dhiraj K. Pradhan, University of Bristol; Serkan Askar, Maciej Ciesielski, University of Massachusetts, Amherst

11:50-1:00pm Lunch

Session 8 1:00-1:50pm *Behavioral/System-Level Test Case Generation*

High-Level Test Generation for Hardware Testing and Software Validation
Speakers to include: O. Golubeva, M. Sonza Reorda, M. Violante, Politecnico di Torino

Scheduling of Transactions in System-Level Test-Case Generation
Speakers to include: Roy Emek, Yehuda Naveh, IBM Research Lab at Haifa

1:50-2:15pm Break

Session 9 2:15-3:30pm *Comparisons and Evaluations*

A Comparison of BDDs, BMC, and Sequential SAT for Model Checking.
Speakers to include: G. Parthasarathy, M.K Iyer, Li-C. Wang, K-T.Cheng, University of California, Santa Barbara

Genetic Algorithms: the Philosopher's Stone or an Effective Solution for High-level TPG?
Speakers to include: Alessandro Fin, Franco Fummi, Università di Verona

A Method for the Evaluation of Behavioral Fault Models
Speakers to include: Emilio Gaudette, Michael Moussa, University of Massachusetts, Amherst; Ian G. Harris, University of California, Irvine

3:30-4:00pm Break

Session 10 4:00-5:30pm *Panel — "What's the Next 'Big Thing' in Simulation-Based Verification?"*

Organizers: Moshe Levinger and Avi Ziv, IBM Research Lab at Haifa
Panelists to include: Brian Bailey, Mentor Graphics; William H. Joyner, SRC; Yaron Kishai, Verisity, Inc.

For more information, please visit the HLDVT website:

<http://www.hldvt.com/03/>

HLDVT '03

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advance program

IEEE International High Level Design Validation and Test Workshop
 5305 Spine Rd., Ste A
 Boulder, CO 80301

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Hotel Description/Transportation

Downtown luxury hotel on San Francisco Bay in the Financial District across from the Ferry Building, part of the dynamic 8-block Embarcadero Center, convenient to Fisherman's Wharf, Chinatown, Moscone Convention Center, Ghirardelli Square, North Beach and Union Square. Adjacent to all forms of transportation - BART (Bay Area Rapid Transit), Muni intra-city transit, and California Street Cable Car.

For more information, visit the hotel website at <http://sanfranciscoregency.hyatt.com>.

Hotel Directions from Airport

The Hyatt Regency San Francisco is conveniently located in the heart of downtown San Francisco, with easy access by car or public transit. The closest airport is San Francisco International (SFO), about 20 minutes to the south.

HLDVT'03 Workshop Registration Form

Mail or fax this form to:
HLDVT'03
 5305 Spine Rd., Ste. A
 Boulder, CO 80301 USA • Tel (303) 530-4562 • Fax (303) 530-4334

First Name _____ Last Name _____ Company _____
 Mail Stop _____ Street Address _____ City _____ State _____ Zip _____
 Country _____ Phone _____ Fax _____
 Email _____ IEEE Member# _____ Dietary Requirements Vegetarian _____ Other _____

Advance Registration (Postmarked by October 15, 2003)

	IEEE Member	Non-Member	IEEE Student Member	Student Non-Member
Pre-Registration	\$375	\$475	\$250	\$310
After Oct.15	\$475	\$595	\$300	\$375
Additional meal charges for companion @ \$150 _____ TOTAL FEES _____				

Send full payment in U.S. dollars with this form. Use a **check drawn on a US bank or a major credit card**. For payments from non-US banks the attendee will be charged a collection fee of \$30.00. Purchase orders are not accepted.

Make checks payable to **IEEE HLDVT'03**. Use your credit card if registering by fax.

Check _____ Visa _____ Mastercard _____ American Express _____ Card # _____ Exp. date _____

Name (as it appears on card) _____ Signature _____

I agree to pay the total amount according to the card issuer agreement.

Refunds: Requests for refunds received before October 15, 2003 will be subject to a \$50 processing fee. No refunds will be made for cancellations received after October 15, 2003 and all registration fees will be forfeited. Attendance is limited. Register early to avoid disappointment. No registrations will be accepted after October 20, 2003, in the HLDVT office. After October 20, 2003, there will be on-site registration only.

HLDVT'03 Hotel Registration Form

Register before October 22, 2003 for the HLDVT'03 Workshop of \$159 (single) or \$159 (double). Hotel space is limited. Please register before October 22, 2003 to avoid disappointment.

Mail or fax this form to:
 Hyatt Regency San Francisco
 5 Embarcadero Center
 San Francisco, California
 Tel: (415) 788-1234 Fax: (415) 398-2567

Hotel cancellation policy is 24 hours prior to arrival

First Name _____ Last Name _____ Company _____
 Mail Stop _____ Street Address _____ City _____ State _____ Zip _____
 Country _____ Phone _____ Fax _____

Hotel rates - single..... \$159.00 double..... \$159.00

Arrival Date _____ Departure Date _____

Your reservation can be guaranteed by credit card. Your credit card will be billed for first night's deposit.

Check _____ Visa _____ Mastercard _____ American Express _____ Card # _____ Exp. date _____

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HLDVT'03 is sponsored by the IEEE Computer Society Test Technology Technical Council and the IEEE Computer Society Design Automation Technical Committee.

