



Nanotechnology: System Level Issues

System Design

Grains of Salt

Forecast

Quantum Scale Memory



Physical System Hierarchy



- ◆ Coherence Scale
 - Maintenance of State – latency vs. memory size
- ◆ Clocking Scale
 - Synchronous clocking – power vs. jitter vs. period
- ◆ Connection Scale
 - Gate Connectivity – design flexibility vs. connection cost
- ◆ Feedback Scale
 - Scale of complex gates – Flip-Flop Timing Aperture
- ◆ Quantum Scale
 - Scale of coherent quantum state

System Communication

- ◆ Fundamental System Constraint (30+ years)
 - Wires:
 - Diffusive (RC limit) Voltage Signaling
 - Transmission (RLC) Wave Signaling
 - Optical:
 - Transmission (Cut-off at few hundred nm, sensor)
 - Quantum:
 - Thermal Coherence (Limited to small distances)

Grain of Salt

- ◆ Uncertainty Principle:

$$\Delta E \cdot \Delta T > \hbar \quad \Delta p \cdot \Delta x > \hbar \quad (\text{other linked pairs})$$

$$\hbar = 1.05 \times 10^{-34} \text{ Joule} \cdot \text{Second}$$

Examples:

$$20\text{nm CMOS inverter } (1\text{pS}) \cdot (0.005\text{fJ}) = 10^4 \hbar$$

$$1\text{nm Quantum Dot } (10\text{pS}) \cdot (0.32\text{eV}) = 10^4 \hbar$$

Upshot

- ◆ Cannot have high density, low power, high performance at same time
- ◆ Potential barrier leakage (FET sub-threshold slope) is a thermodynamic limitation:
 - No more free reduction of V_{sw}
 - Power dissipation is $I V = C V_{sw} f V_{dd}$
 - FINFET (300K) V_t 0.4V, I_{off} 15nA/ μm , I_{on} 400 $\mu\text{A}/\mu\text{m}$
 - Molecular Switch (300K)
 V_t 0.5-1.0V, I_{off} 13nA, I_{on} 250nA

Forecast

- ◆ Nanotechnology will happen (soon!)
 - But will be integrated in conventional way
- ◆ Shift uncertainty from Error to Latency
 - Nano-memory won't be faulty
 - Cannot predict access time
- ◆ Implicit Computation Model
 - CAM / FFT and other non-dissipative functions can avoid some communication costs.



Quantum Dot Memory

- ◆ DRAM is close to limits (4-7 years)
 - Cell capacity has been constant for 3 generations
 - Leakage scales poorly
 - Already needs deep trench, exotic dielectric
- ◆ Quantum Confined Electron RAM (3-5 years)
 - Few – single electron, leakage dominated by tunneling
 - Density/Power/Delay dominated by CMOS interconnect