

HLDVT'05

WEDNESDAY, NOVEMBER 305:00 pm - 7:30 pm Registration
7:30 pm - 9:30 pm Reception & Buffet Dinner**THURSDAY, DECEMBER 1**7:00 am - 8:00 am Continental Breakfast
7:00 am - 6:00 pm Registration
8:00 am - 8:10 am Welcome Remarks**Session 1****8:10 am - 9:50 am Test, Fault & Error Modeling**Simulation-Based Functional Test Generation for Embedded Processors
Hung-Pin (Charles) Wen, opwen@ece.ucsb.edu, Li-C. Wang, Kwang-Ting Cheng, Univ. of California, Santa Barbara, CA

Scalable Defect Mapping and Configuration of Memory-Based Nanofabrics

Chen He, che@ece.utexas.edu, Univ. of Texas, Freescale Semiconductor, Inc., Austin TX, Margarida F. Jacome, Gustavo de Veciana, Univ. of Texas, Austin, TX

Improvement of Fault Injection Techniques Based on VHDL Code Modification

Joaquin Gracia, jgracia@disca.upv.es, Daniel Gil, Juan C. Baraza, Pedro J. Gil, Universidad Politecnica de Valencia, Valencia, Spain

MVP: A Mutation-Based Validation Paradigm

Jorge Campos, jcampos@ucdavis.edu, Hussain Al-Asaad, Univ. of California, Davis, CA

9:50 am - 10:10 am Break

Session 2**10:10 am - 11:25 am Equivalence Verification**

Establishing Latch Correspondence for Embedded Circuits of PowerPC(R) Microprocessors

Himyanshu Anand, himyanshu.anand@freescale.com, Jayanta Bhadra, Alper Sen, Magdy S. Abadir, Kenneth G. Davis, Freescale Semiconductor Inc., Austin, TX

Sequential Equivalence Checking Based on K-th Invariants and Circuit SAT Solving

Feng Lu, lufeng@ece.ucsb.edu, Tim Cheng, Univ. of California, Santa Barbara, CA

VERISEC: VERifying Equivalence of SEquential Circuits using SAT

Manan Syal, mysal@vt.edu, Intel Corp., Hillsboro, OR, Michael S. Hsiao, Virginia Tech., Blacksburg, VA

11:25 am - 11:45 am Break

Session 3**11:45 am - 12:35 pm System-Level Modeling & Co-Design**

Automated Clock Inference for Stream Function-Based System Level Specifications

Sandeep K. Shukla, shukla@vt.edu, Virginia Tech., Blacksburg, VA, Jean-Pierre Talpin, IRISA/INRIA, Rennes, France

Cosimulation of ITRON-Based Embedded Software with SystemC

Shin-ichiro Chikada, chikada@ertl.jp, Shinya Honda, Hiroyuki Tomiyama, Hiroaki Takada, Nagoya Univ., Aichi, Japan

12:35 pm - 2:00 pm Lunch

Session 4**2:00 pm - 3:15 pm Validation Test Generation I**A Software Test Program Generator for Verifying System-on-Chips
Adriel Cheng, acheng@eleceng.adelaide.edu.au, Atanas Parashkevov, Cheng-Chev Lim, The Univ. of Adelaide, Adelaide, SA, Australia

Stimulus Generation for Interface Protocol Verification Using the Non-Deterministic Extended Finite State Machine Model

Che-Hua Shih, matar@eda.ee.nctu.edu.tw, Juinn-Dar Huang, Jing-Yang Jou, National Chiao Tung Univ., Hsinchu, Taiwan, ROC

A Test Generator for the Transmeta Efficcon VLIW Processor

Kevin D. Rich, kdrich@transmeta.com, Shankar Govindaraju, Robert Shaw, David Dobrikin, Transmeta Corp., Santa Clara, CA

3:15 pm - 3:35 pm Break

Session 5**3:35 pm - 4:25 pm Validation Test Generation II**

Reuse in System-Level Stimuli-Generation

Shady Copt, shady@il.ibm.com, Itai Jaeger, Yossi Lichtenstein, Yoav Katz, IBM Haifa Research Labs, Haifa, Israel, Anita Devadasan, Audrey Romonosky, IBM Corp., Austin, TX

Harnessing Machine Learning to Improve the Success Rate of Stimuli Generation

Ari Frueng, arief@il.ibm.com, Shai Fine, Itai Jaeger, Yehuda Naveh, Avi Ziv, IBM Haifa Research Labs, Haifa, Israel, Yishay Mansour, Tel Aviv Univ., Tel Aviv, Israel

4:25 pm - 4:45 pm Break

Session 6**4:45 pm - 6:00 pm New Approaches in Simulation**

A New Simulation-Based Property Checking Algorithm Based on Partitioned Alternative Search Space Traversal

Qingwei Wu, qiwu@cadence.com, Cadence Design Systems, Inc., San Jose, CA, Michael S. Hsiao, Virginia Tech., Blacksburg, VA

Validating Families of Latency Insensitive Protocols

Syed Suhaib, ssuhaib@vt.edu, Deepak Mathaikutty, Sandeep Shukla, Virginia Tech., Blacksburg, VA, David Berner, INRIA-IRISA, France

GASIM: A Fast Galois Field Based Simulator for Functional Model

Ashutosh Kumar Singh, ashutosh@unitar.edu.my, UNITAR, Selangor Darul Ehsan, Malaysia, Dhiraj K. Pradhan, Univ. of Bristol, Bristol, United Kingdom, T.L. Rajaprabhu, Georgia Institute of Tech., Atlanta, GA, Abusaleh M. Jabir, Oxford Brookes Univ., Oxford, United Kingdom**FRIDAY, DECEMBER 2**

7:00 am - 12:00 pm Registration

7:00 am - 8:00 am Continental Breakfast

Session 7**8:00 am - 9:40 am Formal Verification**

Overlap Reduction in Symbolic System Traversal

Prakash Mohan Perariandam, prakash@informatik.uni-tuebingen.de, P.K. Nalla, R.J. Weiss, J. Ruf, T. Kropf, W. Rosenstiel, Univ. of Tuebingen, Tuebingen, Germany

Formal Verification of High-Level Conformance with Symbolic Simulation

Armaghan Naik, armaghan.w.naik@intel.com, Intel Corp., Hudson, MA, Roope Kaivola, Intel Corp., Hillsboro, OR

Detailed information can be found on the

HLDVT web site<http://www.hldvt.com/05/>**Session 7 (continued)**

A Method for Generation of GSTE Assertion Graphs

Edward Smith, ed.smith@comlab.ox.ac.uk, Oxford Univ., Oxford, United Kingdom

Automatic Abstraction Refinement for Petri Nets Verification

Zhenyu Chen, zychen@mail.edu.cn, Conghua Zhou, Decheng Ding, Nanjing Univ., China

9:40 am - 10:00 am Break

Session 8**10:00 am - 11:15 am SAT & SAT Applications**

An Optimum Algorithm for Compacting Error Traces for Efficient Design Error Debugging

Chia-Chih Yen, jackr@eda.ee.nctu.edu.tw, Jing-Yang Jou, National Chiao-Tung Univ., Hsinchu, Taiwan

Increasing the Deductibility in CNF Instances for Efficient SAT-based Bounded Model Checking

Vishnu C. Vimjam, vvimjam@vt.edu, Michael S. Hsiao, Virginia Tech., Blacksburg, VA

B-Cubing Theory: New Possibilities for Efficient SAT-Solving

Alan J. Hu, ajh@cs.ubc.ca, Domagoj Babic, Jesse Bingham, Univ. of British Columbia, Vancouver, BC, Canada

11:15 am - 11:35 am Break

Session 9**11:35 am - 12:25 pm Security**

Multi-level Design Validation in a Secure Embedded System

David D. Hwang, dhwang@ee.ucla.edu, Shenglin Yang, Ingrid Verbauwhede, Univ. of California, Los Angeles, CA, Patrick Schaumont, Virginia Tech., Blacksburg, VA

Security Evaluation Against Electromagnetic Analysis at Design Time

Huiyun Li, huiyun.li@cl.cam.ac.uk, Theodore Marketos, Simon Moore, Univ. of Cambridge, Cambridge, United Kingdom

12:25 pm - 1:45 pm Lunch

Session 10**1:45 pm - 3:00 pm Coverage**

Formal Meaning of Coverage Metrics in Simulation-Based Hardware Design Verification

Pablo Sanchez, sanchez@teisa.unican.es, Iñigo Ugarte, Univ. of Cantabria, Cantabria, Spain

Advanced Analysis Techniques for Cross-Product Coverage

Laurent Fournier, laurent@il.ibm.com, Hezi Aztachi, Avi Ziv, Keren Zohar, IBM Haifa Research Labs, Haifa, Israel

A Proof of Correctness for the Construction of Property Monitors

Katell Morin-Allory, katell.morin-allory@imag.fr, Dominique Borriane, Tima Labs. Grenoble, Cedex, France

3:00 pm - 3:20 pm Break

Session 11**3:20 pm - 5:00 pm Panel — "Functional Coverage: Is Your Design Exposed?"**

Moderator: Andrew Piziali - Cadence Design Systems, Verification Application Specialist, Plano, TX

Panelists: Neyaz Khan - Cadence Design Systems, Plano, TX
Laurent Fournier - IBM, Haifa, Israel
Gery Osowiecki - Texas Instruments, Plano, TX
Tom Anderson - Synopsys, San Jose, CA
Michael Bair - Intel, Hillsboro, OR

HLDVT '05

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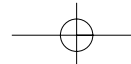
Sandeep Shukla, Virginia Tech.

Miroslav Velez, Reservoir Labs

Li-C. Wang, UC Santa Barbara

Jin Yang, Intel Corp.

Advance Program



Hotel Description/Transportation

Conveniently located at the gateway to California's renowned Napa Wine Country, the Marriott Napa Valley Hotel & Spa offers the perfect setting. Situated just off Highway 29, our hotel is accessible to the full range of local attractions and three major airports. For more information, visit the hotel website at <http://www.napavalleymarriott.com/>

Hotel Directions from Airport

From San Francisco Airport (60 mi NE): Take Highway 101 North to 80 East. Cross the Bay Bridge. Follow signs to Sacramento. Exit onto Highway 37. Turn right on Highway 29 North. Turn left at Redwood Road. Turn right on Solano Avenue.
 From Oakland Airport (50 mi N): Take Highway 880 North to 980, to 580 West, to 80 East (Sacramento). Exit Highway 37. Turn right on Highway 29 North. Turn left onto Redwood Road. Turn right on Solano Avenue.

IEEE International High Level Design Validation and Test Workshop
 5405 Spine Rd., Ste 102
 Boulder, CO 80301

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HLDVT'05 Workshop Registration Form

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 5405 Spine Rd., Ste. 102
 Boulder, CO 80301 USA • Tel 303-530-4562 • Fax 303-530-4334
 email: register@mpassociates.com

First Name _____ Last Name _____ Company _____
 Mail Stop _____ Street Address _____ City _____ State _____ Zip _____
 Country _____ Phone _____ Fax _____
 Email _____ IEEE Member# _____ Student # _____
 Dietary Requirements Vegetarian _____ Other _____

Advance Registration (Postmarked by October 18, 2005)

	IEEE Member	Non-Member	Student Member	Student Non-member
Pre-Registration	\$375	\$475	\$250	\$310
After Oct. 18	\$475	\$595	\$300	\$375

Additional meal charges for companion @ \$150 _____ **TOTAL FEES** _____

Send full payment in U.S. dollars with this form. Use a **check drawn on a US bank or a major credit card**. For payments from non-US banks the attendee will be charged a collection fee of \$30.00. Purchase orders are not accepted. Make checks payable to **IEEE HLDVT'05**. Use your credit card if registering by fax.

Check _____ Visa _____ Mastercard _____ American Express _____ Card # _____ Exp. date _____
 Name (as it appears on card) _____ Signature _____
I agree to pay the total amount according to the card issuer agreement.

Refunds: Requests for refunds received before November 11, 2005 will be subject to a \$25 processing fee. No refunds will be made for cancellations received after November 11, 2005 and all registration fees will be forfeited. Attendance is limited. Register early to avoid disappointment. No registrations will be accepted in the HLDVT office after November 21, 2005. After November 21, 2005, there will be on-site registration only.

HLDVT'05 Hotel Registration Form

Register before Wednesday, November 9, 2005 for the HLDVT'05 discounted room rate of \$89 (single) or \$109 (double). Hotel space is limited. Please register before November 9, 2005 to avoid disappointment.

Mail or fax this form to:
 Napa Valley Marriott Hotel
 3425 Solano Avenue
 Napa, CA, 94558, USA
 Phone: 707-253-8600 Fax: 707-258-1320
www.napavalleymarriott.com

Should guests cancel a reservation, deposits will be refunded by the Hotel if notice is received prior to 6:00 pm on the date of arrival.

First Name _____ Last Name _____ Company _____
 Mail Stop _____ Street Address _____ City _____ State _____ Zip _____
 Country _____ Phone _____ Fax _____

Hotel rates - single..... \$89.00 double..... \$109.00

Arrival Date _____ Departure Date _____
 Your reservation can be guaranteed by credit card. Your credit card will be billed for first night's deposit.
 Check _____ Visa _____ Mastercard _____ American Express _____ Card # _____ Exp. date _____
 Name (as it appears on card) _____ Signature _____
I agree to pay the total amount according to the card issuer agreement.

ADVANCE PROGRAM

HLDVT'05

Tenth Annual IEEE International Workshop on High Level Design Validation and Test

November 30-December 2, 2005
 Napa Valley Marriott, Napa Valley, CA

HLDVT'05 is sponsored by the IEEE Computer Society Test Technology Technical Council and the IEEE Computer Society Design Automation Technical Committee.

