

# Call for Papers

## HLDVT'06

### IEEE International High-Level Design, Validation and Test Workshop Hyatt Regency Monterey, Monterey, California, Nov. 8–10, 2006

#### Organizing Committee

##### *General Chair*

Robert Jones, Intel

##### *Program Chair*

Michael Hsiao, Virginia Tech

##### *Past Chair*

Ian Harris, UC Irvine

##### *Finance*

Yatin Hoskote, Intel

##### *Publicity*

Laurent Fournier, IBM

##### *Local Arrangements*

Vijay Nagasamy, Crimson

##### *Webmaster*

Ismet Bayraktaroglu, Sun

#### Program Committee

Mark Aagaard, Univ. of Waterloo

Jacob Abraham, Univ. of Texas

Hussain Al-Asaad, UC Davis

Felice Balarin, Cadence Berkeley Labs

Valeria Bertacco, Univ. of Michigan

Annette Bunker, Utah State Univ.

Tim Cheng, UC Santa Barbara

Scott Davidson, Sun

Farzan Fallah, Fujitsu Labs of America

Masahiro Fujita, Univ. of Tokyo

Franco Fummi, Univ. di Verona

Kiyoharu Hamaguchi, Osaka Univ.

John Hayes, Univ. of Michigan

Alan Hu, Univ. British Columbia

Ed McCluskey, Stanford Univ.

Naran Narasimhan, Intel

Alex Orailoglu, UC San Diego

Wolfgang Rosenstiel, Tübingen Univ.

Sandeep Shukla, Virginia Tech

Li-C. Wang, UC Santa Barbara

Jin Yang, Intel

#### Steering Committee

Bernard Courtois, TIMA

Sujit Dey, UC San Diego

Prab Varma, Blue Pearl Software

HLDVT 2006 is the eleventh in a series of annual workshops designed to bring together a community of researchers in the areas of design, validation, and test. The workshop revolves around a common theme of addressing the integration of multiple functions on-chip at higher levels of design abstraction, and the techniques and methodologies for modeling, analyzing, and validating such systems. In particular, the workshop has become a unique forum in recent years for researchers and practitioners to discuss the practical issues associated with simulation and validation of extremely large designs. Topics of interest include:

- Simulation-Based Validation
- Formal Verification
- Design Abstraction & Behavioral Modeling
- Error Trace Interpretation & Debugging
- Hybrid SAT/BDD/ATPG Methods
- On-Chip and Core-Based Testing
- Test Generation for Defects, Design Errors, and Delay
- Design/Synthesis for Test
- Hardware/Software Co-Validation
- Emulation and Prototyping

The Program Committee invites authors to submit papers not to exceed 8 pages (10pt minimum font size, reasonable margins and line spacing) describing original and unpublished work. On the title page, please indicate: paper title, name and affiliations of all authors, and the topic category. Also identify a contact author and provide complete mailing address, phone number, fax number and an e-mail address. Panel proposals are also invited. All submissions must be made electronically in PDF or Postscript format using the paper submission webpage: <http://www.hldvt.com/submissions>

Please ensure that your PDF or Postscript file is readable by Acrobat Reader or Ghostview. The submission of an paper or panel proposal will be considered evidence that upon acceptance, the author(s) will present their paper or organize their panel at the workshop.

Submission deadline: **June 16, 2006**

Notification: **August 7, 2006**

Final manuscript: **September 13, 2006**

Authors of selected HLDVT'06 papers will be invited to submit extended versions for a special issue of ACM Transactions on Design Automation of Electronic Systems, to be published in 2007.

Additional information are available at <http://www.hldvt.com/06>

Questions regarding paper submissions and the program may be addressed to the program chair: Michael Hsiao, [programchair@hldvt.com](mailto:programchair@hldvt.com). Other questions may be addressed to the general chair: Robert Jones, [generalchair@hldvt.com](mailto:generalchair@hldvt.com).

HLDVT 2006 is sponsored by the IEEE Computer Society Test Technology Technical Council and the IEEE Computer Society Design Automation Technical Committee. HLDVT 2006 receives corporate support from IBM.