

# HLDVT'06

WEDNESDAY, NOVEMBER 8

6:00 pm - 8:00 pm Registration

THURSDAY, NOVEMBER 9

7:00 am - 8:00 am Continental Breakfast

7:00 am - 5:00 pm Registration

8:00 am - 8:10 am Welcome Remarks

8:10am - 9:25am

## Session 1 Test Case Generation I

**DVGen: Increasing Coverage by Automatically Combining Test Specifications**

K. D. Rich, R. Shaw, S. G. Govindaraju, D. Dobrikin, Transmeta Corp.

**Test Directive Generation for Functional Coverage Closure Using**

**Inductive Logic Programming**

H.-W. Hsueh, K. Eder, U. of Bristol

**Automated Coverage Directed Test Generation Using Cell-Based Genetic Algorithm**

A. Samarah, A. Habibi, S. Tahar, Concordia U

9:25am - 9:45am Break

## Session 2: Special Session I

9:45am - 11:00am

**Disjunctive Transition Relation Decomposition for Efficient Reachability Analysis**

S. Stergiou, Stanford U

J. Jain, Fujitsu Labs

**Trends in Test: Challenges and Techniques**

W. Meyer, Synopsys

**Formal Verifications in Modern Chip Designs**

K.-Y. Khoo, Cadence

11:00am - 11:20am Break

## Session 3: Testing and Design for Testability

11:20am - 12:25pm

**DFT and Probabilistic Testability Analysis at RTL**

J. M. Fernandes, M. Santos, A. Oliveira, J. P. Teixeira, IST/INESC-ID

**Easily Testable Implementation for Bit Parallel Multipliers Over GF(2^m)**

H. Rahaman, J. Mathew, A. Jabir, D. K. Pradhan, U. Bristol

**Error Detection Using Model Checking vs. Simulation (short)**

S. Verma, P. Lee, I. Harris, U California, Irvine

12:25pm - 2:00pm Lunch

## Session 4: Assertions and Transactions

2:00pm - 3:40pm

**Assertion-based Verification of Behavioral Descriptions with Non-linear Solver**

I. Ugarte, P. Sanchez, U. Cantabria

**Efficient Automata-Based Assertion-Checker Synthesis of PSL Properties**

M. Boule, Z. Zilic, McGill U

**Specification Language for Transaction Level Assertions**

W. Echer, V. Esen, M. Hull, T. Steining, M. Velten, Infineon

**On the Automatic Transactor Generation for the TLM-based Design Flow**

N. Bombieri, F. Fummi, U. Verona

3:40pm - 4:00pm Break

## Session 5: Test Case Generation II

4:00pm - 5:40pm

**Addressing Test Generation Challenges for Configurable Processor Verification**

S. Johnson, D. Jani, Tensilica

M. Rimon, Y. Lichtenstein, A. Adir, I. Jaeger, M. Vinov, IBM Corp.

**DeepTrans - Extending the Model-based Approach to Functional Verification of Address Translation Mechanisms**

A. Koyfman, Y. Katz, A. Adir, L. Fournier, IBM

**CP with Architectural State Lookup for Functional Test Generation**

B. Gutkovich, A. Moss, Intel

**Reusable On-Chip System Level Verification for Simulation Emulation and Silicon**

A. Maman, S. Goldschlager, H. Miller, D. Bell, R. Slater, O. Ben-Moshe, N. Levi, H. Gilboa, Freescale

## Keynote: J. Scott Runner, Qualcomm

6:00pm - 8:00pm Dinner Banquet

**Title: Time to Quality: The Challenge of Verification Efficiency**

FRIDAY, NOVEMBER 10

7:00 am - 8:00 am Continental Breakfast

7:00 am - 12:00 pm Registration

## Session 6: Transformation-based Verification

8:00am - 9:05am

**Transaction Routing and its Verification by Correct Model Transformations**

S. Abdi, D. Gajski, U California, Irvine

**Taming the Complexity of STE-based Design Verification Using Program Slicing**

V. Vedula, F. Andersen, J. Abraham, U Texas, Austin

**MMV: Metamodeling Based Microprocessor Validation Environment (short)**

A. T. Dingankar, Intel

D. Mathaikutty, S. Shukla, Virginia Tech

S. Kodakara, D. Lijja, U. Minnesota

9:05am - 9:25am Break

Detailed information can be found on the

**HLDVT web site**

<http://www.hldvt.com/06/>

## Session 7: Special Session II

9:25am - 10:40am

**Distance-Guided Hybrid Verification with GUIDO**

V. Bertacco, U Michigan

**EverLost: A Flexible Platform for Industrial-Strength Abstraction-Guided Simulation**

A. Hu, U British Columbia

**Semi-Formal Verification at IBM**

J. Baumgartner, IBM Corp.

10:40am - 11:00am Break

## Session 8: SAT and Equivalence Verification

11:00am - 12:30pm

**Guiding CNF-SAT Search by Analyzing Constraint-Variable Dependencies and Clause Lengths**

V. Durairaj, P. Kalla, U Utah

**Equivalence Checking with Rule-Based Equivalence Propagation and High-Level Synthesis**

T. Nishihara, T. Matsumoto, M. Fujita, U Tokyo

**Practical Issues in Sequential Equivalence Checking through**

**Alignability: Handling Don't Cares and Generating Debug Traces**

I.-H. Moon, P. Bjesse, C. Pixley, Synopsys

**IChecker: An Efficient Checker for Inductive Invariants (short)**

F. Lu, T. Cheng, U California, Santa-Barbara

12:30 - 2:00 Lunch

## Session 9: Panel: Assertion-Based Verification - What is the Big Deal?

2:00pm - 3:30pm

**Organizer: S. Shukla, Virginia Tech.**

**Moderator: A. Hu, U. British Columbia**

**Panelists: TBD**

3:30pm - 3:50pm Break

## Session 10: System Level View and Modeling

3:50pm - 5:20pm

**Runtime Deadlock Analysis of SystemC Design**

E. Cheung, P. Satapathy, V. Pham, H. Hsieh, U California, Riverside

X. Chen, Novas

**Extracting a simplified view of design functionality via vector simulation**

O. Guzey, C. H.-P. Wen, L.-C. Wang, U California, Santa-Barbara

T. Feng, Cadence, M. Abadir, Freescale

**A Tool for Automatic Detection of Deadlock in Wormhole Networks on Chip**

S. Taktak, J.-L. Desbarbieux, U Paris 6

E. Encrenaz, ENS Cachan & CNRS

**Polychronous Methodology for System Design: A True Concurrency Approach (short)**

S. Suhaib, D. Mathaikutty, S. Shukla, Virginia Tech

J.-P. Talpin, INRIA

HLDVT '06

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# Advance Program

### Hotel Description/Transportation

Experience a hidden gem at Hyatt Regency Monterey. Play a round on Pebble Beach Company's championship Del Monte Golf Course, or perhaps a tennis lesson and game is more your style. Take a dip in the pools, followed by a pampering massage. Enjoy a wide array of dining choices in our luxury hotel in Monterey – including our famous sports bar. You'll delight in the deluxe amenities and unmatched service that await you at our Monterey, California hotel. For more information, visit the hotel website at <http://monterey.hyatt.com/>

### Hotel Directions from Airport

From Monterey Peninsula Airport (1 1/2 miles): Turn right on Garden Road, left on Mark Thomas Dr. Hotel is on left.

From Interstate 5 (either North- or Southbound) - take Highway 152 West (towards Gilroy). At Highway 101, turn South (whether you are North- or Southbound) and follow above directions as from San Francisco/San Jose. From Highway 680 or 880 (East Bay area) - take Highway 680 or 880 towards San Jose until you reach 101 South. Follow above directions as from San Francisco/San Jose.

### HLDVT'06 Workshop Registration Form – register on-line [www.hldvt.com/06/](http://www.hldvt.com/06/)

Mail or fax this form to:

**HLDVT'06**  
5405 Spine Rd., Ste. 102  
Boulder, CO 80301 USA • Tel 303-530-4562 • Fax 303-530-4334  
email: [register@mpassociates.com](mailto:register@mpassociates.com)

First Name \_\_\_\_\_ Last Name \_\_\_\_\_ Company \_\_\_\_\_  
 Mail Stop \_\_\_\_\_ Street Address \_\_\_\_\_ City \_\_\_\_\_ State \_\_\_\_\_ Zip \_\_\_\_\_  
 Country \_\_\_\_\_ Phone \_\_\_\_\_ Fax \_\_\_\_\_  
 Email \_\_\_\_\_ IEEE Member# \_\_\_\_\_ Student # \_\_\_\_\_  
 Dietary Requirements Vegetarian \_\_\_\_\_ Other \_\_\_\_\_

### Advance Registration (Postmarked by October 19, 2006)

	IEEE Member	Non-Member	Student Member	Student Non-member
<b>Pre-Registration</b>	<b>\$395</b>	<b>\$495</b>	<b>\$250</b>	<b>\$310</b>
<b>After Nov. 11</b>	<b>\$495</b>	<b>\$595</b>	<b>\$350</b>	<b>\$410</b>

Additional meal charges for companion @ \$150 **TOTAL FEES** \_\_\_\_\_

Send full payment in U.S. dollars with this form. Use a **check drawn on a US bank or a major credit card**. For payments from non-US banks the attendee will be charged a collection fee of \$30.00. Purchase orders are not accepted. Make checks payable to **IEEE HLDVT'06**. Use your credit card if registering by fax.

Check \_\_\_\_\_ Visa \_\_\_\_\_ Mastercard \_\_\_\_\_ American Express \_\_\_\_\_ Card # \_\_\_\_\_ Exp. date \_\_\_\_\_  
 Name (as it appears on card) \_\_\_\_\_ Signature \_\_\_\_\_  
I agree to pay the total amount according to the card issuer agreement.

**Refunds:** Requests for refunds received before October 19, 2006, will be subject to a \$25 processing fee. No refunds will be made for cancellations received after October 19, 2006, and all registration fees will be forfeited. Attendance is limited. Register early to avoid disappointment. No registrations will be accepted in the HLDVT office after October 28, 2006. After October 28, 2006, there will be on-site registration only.

### HLDVT'06 Hotel Registration Form

**Register before Tuesday, October 23, 2006, for the HLDVT'06 discounted room rate. Hotel space is limited. Please register before October 23, 2006, to avoid disappointment.**

Mail or fax this form to:

Hyatt Regency Monterey  
1 Old Golf Course Road,  
Monterey, California, USA 93940-4908  
Tel: 831 372 1234 Fax: 831 375 3960

Should guests cancel a reservation, deposits will be refunded by the Hotel if notice is received prior to 6:00 pm on the date of arrival.  
Register on-line: HLDVT Group Code: G-IECS  
<http://monterey.hyatt.com/>

First Name \_\_\_\_\_ Last Name \_\_\_\_\_ Company \_\_\_\_\_  
 Mail Stop \_\_\_\_\_ Street Address \_\_\_\_\_ City \_\_\_\_\_ State \_\_\_\_\_ Zip \_\_\_\_\_  
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**Hotel rates - single/double deluxe.... \$145.00 triple deluxe..... \$160.00 quad deluxe..... \$175.00**

Arrival Date \_\_\_\_\_ Departure Date \_\_\_\_\_  
 Your reservation can be guaranteed by credit card. Your credit card will be billed for first night's deposit.

Check \_\_\_\_\_ Visa \_\_\_\_\_ Mastercard \_\_\_\_\_ American Express \_\_\_\_\_ Card # \_\_\_\_\_ Exp. date \_\_\_\_\_  
 Name (as it appears on card) \_\_\_\_\_ Signature \_\_\_\_\_  
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### IEEE International High Level Design Validation and Test Workshop

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# ADVANCE PROGRAM

## HLDVT'06

Eleventh Annual IEEE International Workshop on High Level Design Validation and Test

November 8-10, 2006  
Hyatt Regency Monterey, Monterey, CA



HLDVT'06 is sponsored by the IEEE Computer Society Test Technology Technical Council and the IEEE Computer Society Design Automation Technical Committee.

