

HLDVT'08

WEDNESDAY, November 19

6:00 - 8:00pm

Registration

THURSDAY, November 20

7:30am - 5:00pm

Registration

7:30 - 8:20am

Continental Breakfast

8:20 - 8:30am

Welcome Address

Session 1: SOC Verification Methodologies

8:30 - 9:45am

Positioning Test-Benches and Test-Programs in Interaction-Oriented System-on-Chip Verification

Xiaoxi Xu, Cheng-Chew Lim and Michael Liebelt - Univ. of Adelaide, Australia

A Method for Hunting Bugs that Occur Due to System Conflicts

Daniel Geist and Oded Vaida - Intel Corp., Haifa, Israel

Applications of Observer and Decorator Design Patterns in SoC Verification

Farzin Karimi - Metronome, Inc.

9:45 - 10:00am

Break

Session 2: Test

10:00 - 10:50am

A BIST Scheme for Full Characterization of ADC Parameters in Mixed-Signal SoCs

Chao Yuan, Yuanfu Zhao and Jun Du - Beijing Microelectronics Technology Institute

Test Slice Difference Technique for Low Power Encoding

Wei-Lin Li, Tsung-Tang Chen, Po-Han Wu and Jiann-Chyi Rau - Tamkang Univ., Taiwan R.O.C.

10:50 - 11:00am

Break

Session 3: Panel - Software Practices for Verification/Testbench Management

11:00am - 12:30pm

Moderator: Shireesh Verma - Conexant Systems, Inc.

Panelists:

Mark Glassar - Mentor Graphics, Inc.

Badri Gopalan - Synopsys, Inc.

Srinath Atluri - Cisco Systems, Inc.

Sharon Rosenberg - Cadence Design Systems

Valeria Bertacco - Univ. of Michigan

12:30 - 2:00pm

Lunch

Session 4: Formal Verification

2:00 - 3:40pm

On Dynamic Switching of Navigation for Semi-Formal Design

Ankur Parikh and Michael Hsiao - Virginia Tech., USA

Multi-Level Bounded Model Checking to Detect Bugs Beyond the Bound

Tasuku Nishihara, Takeshi Matsumoto and Masahiro Fujita - Univ. of Tokyo

Proving and Disproving Assertion Rewrite Rules by Automated Theorem Proving

Katell Morin-Allory - TIMA, France, Marc Boulé - McGill Univ., Canada
Dominique Borrione - TIMA, France, Zeljko Zilic - McGill Univ., Canada

Janus: A Novel Use of Formal Verification to do Targeted

Behavioral Equivalence

Prakash Math and David Hoenig - Intel Corp., Hillsboro, OR, USA

3:40 - 3:55pm

Break

Session 5: Invited Session: On-Chip Instrumentation for Silicon Validation and Debug

3:55 - 5:55pm

In-System Silicon Validation Using a Reconfigurable Platform

Miron Abramovici - DAFCA

On-Chip Instrument Application to SoC Analysis

Neal Stollon - HDL Dynamics, Inc.

Banquet Dinner and Keynote Address:

7:00 - 10:00pm

Keynote Speaker: TBD

FRIDAY, November 21

7:00am - 12:30pm

Registration

7:00 - 8:00am

Continental Breakfast

Session 6: Functional Testing and Verification

8:00 - 9:40am

Test and Validation of a Non-Deterministic System - True Random

Number Generator

Kapila Udawatta, Sergey Maidanov, Mehdi Ehsanian and Surya Musunuri - Intel Corp.

Functional Testing Approaches for BIFST-able tlm_fifo

Homa Alemzadeh - Univ. of Tehran, Iran
Stefano Di Carlo, Alberto Scionti and Paolo Prinetto - Politecnico de Torino, Italy
Zainalabedin Navabi - Univ. of Tehran, Iran

IBM System z Functional and Performance Verification Using X-Gen

Torsten Schober, Shimon Landa, Bodo Hoppe and Ronny Morad - IBM Corp.

Timing Verification of Distributed Network Systems at Higher Levels of Abstraction

Hassan Hatefi-Ardakani, Amir Masoud Gharehbaghi and Shaahin Hessabi - Sharif Univ. of Technology, Tehran

9:40 - 9:50am

Break

Session 7: Simulation

9:50 - 11:05am

Temporal Parallel Gate-level Timing Simulation

Dusung Kim and Maciej Ciesielski - Univ. of Massachusetts, Amherst
Kyuho Shim and Seiyang Yang - Pusan National Univ., Korea

The Role of Parallel Simulation on Functional Verification

Giuseppe Di Guglielmo, Franco Fummi - Univ. of Verona, Italy

Mark Hampton - Certess, France

Graziano Pravaddelli and Francesco Stefanni - Univ. of Verona, Italy

A HW/SW Co-Simulation Framework for the Verification of Multi-CPU Systems

Stefano Cordibella, Franco Fummi, Giovanni Perbellini and Davide Quaglia - Univ. of Verona, Italy

11:05 - 11:15am

Break

Session 8: Panel - SoC Power Management Implications on Validation and Testing

11:15am - 12:35pm

Moderator: Bhanu Kapoor - Mimasac

Panelists:

John Goodenough - ARM

Manuel A d'Abreu - Sandisk Corp.

Shireesh Verma - Conexant Systems, Inc.

Kaushik Roy - Purdue Univ.

Shankar Hemmady - Synopsys, Inc.

12:35 - 2:00pm

Lunch

Session 9: Special Session: What's So Intelligent about Testbenches?

2:00 - 3:30pm

Organizer: Avi Ziv - IBM Corp.

Automatic Test Generation for Coverage Improvement

Chris Wilson - Nusym Technology, Inc.

Capturing Functional Intent in Intelligent Testbenches

Adnan Hamid - Breker Verification Systems

Why Intelligent Verification Needs Functional Qualification

Joerg Grosse - Certess

3:30 - 3:40pm

Break

Session 10: Coverage and Metrics

3:40 - 4:30pm

Optimized Coverage-Directed Random Simulation

Inigo Ugarte and Pablo Sanchez - Univ. of Cantabria, Spain

Evaluation of an Efficient Control-Oriented Coverage Metric

Kiran Ramineni, Shireesh Verma and Ian Harris - Univ. of California, Irvine

4:30 - 4:40pm

Break

Session 11: Defect and Fault Models and Test

4:40 - 5:55pm

High-Level Vulnerability over Space and Time to Insidious Soft Errors

Kenneth Zick and John Hayes - Univ. of Michigan

Automating Defects Simulation and Fault Modeling for SRAMs

Stefano Di Carlo, Paolo Prinetto and Alberto Scionti - Politecnico de Torino, Italy
Zaid Al-Ars - Delft Univ. of Technology, The Netherlands

Injecting Intermittent Faults for the Dependability Validation of Commercial Microcontrollers

Daniel Gil, Luis J. Saiz, Joaquin Gracia, Juan C. Baraza and Pedro Gil - Univ. Politecnica de Valencia, Spain

HLDVT '08

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Advance Program

Detailed information can be found on the

HLDVT website

<http://www.hldvt.com/08/>

Hotel Description/Transportation

Discover an alpine paradise at Hyatt Regency Lake Tahoe Resort, Spa and Casino. Nestled within the Sierra Mountain Range, the stunning locale of this Four Diamond Lake Tahoe hotel is the ideal setting for year-round pampering. Take a cruise on one of our private boats, then tempt Lady Luck in the Casino. Ease tired muscles with a deep-tissue massage in our world-class spa, or bask in the sunshine on the private beach. For more information, visit the hotel website at <http://www.laketahoe.hyatt.com/>

Hotel Directions from Airport

From San Francisco (200 miles) Sacramento (115 miles) Take 80 East toward Reno. Take exit 188B off I-80, to CA-267 toward Sierraville/Lake Tahoe. At the end of off-ramp, turn right on CA-267/Truckee Bypass. Turn left onto CA-28 and follow this through the California/Nevada border. Turn right onto Lakeshore Blvd. Turn left onto Country Club Drive. Hotel is on the left hand side at the corner of Country Club Drive and Lakeshore Blvd.

HLDVT'08 Workshop Registration Form – register online www.hldvt.com/08/

Mail or fax this form to:

HLDVT'08
1721 Boxelder St., Ste. 107
Louisville, CO 80027 USA • Tel 303-530-4562 • Fax 303-530-4334
email: register@mpassociates.com

First Name _____ Last Name _____ Company _____
 Mail Stop _____ Street Address _____ City _____ State _____ Zip _____
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 Email _____ IEEE Member# _____ Student # _____
 Dietary Requirements Vegetarian _____ Other _____

Advance Registration (Postmarked by October 16, 2008)

	IEEE Member	Non-member	Student Member	Student Non-member
Pre-Registration	\$440	\$555	\$275	\$325
After Oct. 16	\$555	\$690	\$350	\$395

Guest Banquet Dinner @ \$100 _____ **TOTAL FEES** _____

Send full payment in U.S. dollars with this form. Use a **check drawn on a US bank or a major credit card**. For payments from non-US banks the attendee will be charged a collection fee of \$30.00. Purchase orders are not accepted. Make checks payable to **IEEE HLDVT'08**. Use your credit card if registering by fax.

Check _____ Visa _____ Mastercard _____ American Express _____ Card # _____ Exp. date _____ Sec. Code _____
 Name (as it appears on card) _____ Signature _____
I agree to pay the total amount according to the card issuer agreement.

Refunds: Requests for refunds received before October 16, 2008, will be subject to a \$50 processing fee. No refunds will be made for cancellations received after October 16, 2008, and all registration fees will be forfeited. Faxed or mailed registrations will be accepted through November 7, 2008. Online registration will be accepted through November 14, 2008.

HLDVT'08 Hotel Registration Form

Register online: HLDVT Group Code: G-IEEE
<http://www.laketahoe.hyatt.com/>

Register before **Tuesday, October 16, 2008 at 5:00pm PST**, for the HLDVT'08 discounted room rate. Hotel space is limited. Please register before October 16, 2008, to avoid disappointment.

Mail or fax this form to:

Hyatt Regency Lake Tahoe Resort, Spa and Casino
111 Country Club Drive
Incline Village, Nevada, 89451 USA
Tel: +1 775 832 1234 Fax: +1 775 831 2171

First Name _____ Last Name _____ Company _____
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Hotel rates - Single/Double \$140.00

Cancellation Policy: Individual must cancel 7 days prior to check-in to receive a refund on their deposit. Within 7 days a one night room plus tax fee will be charged to your credit card.

Arrival Date _____ Departure Date _____
 Your reservation can be guaranteed by credit card. Your credit card will be billed for first night's deposit. Sales/room tax is twelve (12%) percent. Resort Services Fee of \$9.
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IEEE International High Level Design Validation and Test Workshop

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ADVANCE PROGRAM

HLDVT'08

IEEE International High Level Design Validation and Test Workshop

November 19-21, 2008

Hyatt Regency Lake Tahoe Resort, Lake Tahoe, NV



HLDVT'08 is sponsored by the IEEE Computer Society Test Technology Technical Council and the IEEE Computer Society Design Automation Technical Committee.

