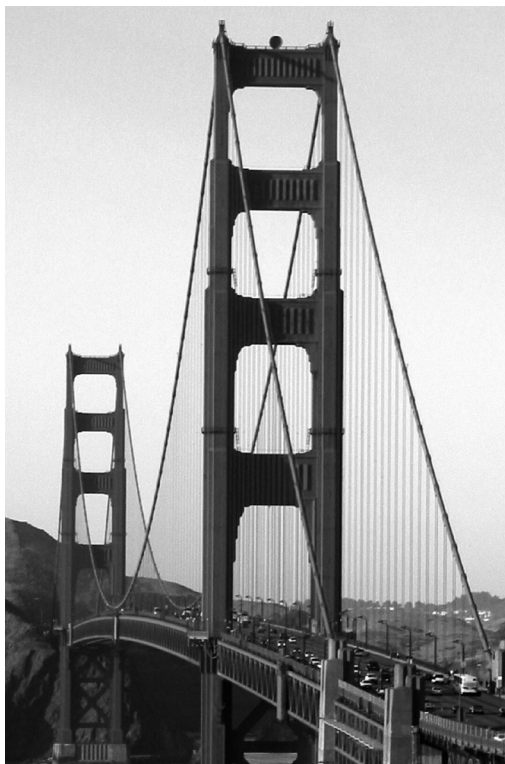


IEEE International High Level Design Validation and Test Workshop  
1721 Boxelder St., Ste. 107  
Louisville, CO 80027 USA

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# HLDVT'09 *Advance Program*

IEEE International High Level Design Validation and Test Workshop



**November 4-6, 2009**  
**Grand Hyatt, San Francisco, CA**

HLDVT'09 is sponsored by the IEEE Computer Society Test Technology Technical Council and the IEEE Computer Society Design Automation Technical Committee.

## November 04, 2009

6:00pm - 8:00pm **Registration**

## November 05, 2009

7:30am - 5:00pm **Registration**

7:30am - 8:20am **Continental Breakfast**

8:20am - 8:35am **Welcome Address**

8:35am - 10:00am

### Session 1: Verification Methodologies and Applications

#### Analysis of Scheduled Latency Insensitive Systems with Periodic Clock Calculus

Bin Xue and Sandeep Shukla - Virginia Tech, USA

#### Exploiting Hierarchical Encodings of Equality to Design Independent Strategies in Parallel SMT Decision Procedures for a Logic of Equality (Short Paper)

Miroslav Velez and Ping Gao - Aries Design Automation, LLC

#### FLARE: a Design Environment for FLASH-based Space Applications (Short Paper)

Maurizio Caramia - Thales Alenia Space Italia, Italy  
Paolo Prinetto, Stefano Di Carlo and Michele Fabiano - Politecnico di Torino, Italy

#### MCBCG: Model Checking Based Sequential Clock-Gating (Short Paper)

Sumit Ahuja and Sandeep Shukla - Virginia Tech, USA

10:00am - 10:15am **Break**

10:15am - 11:05am

### Session 2: Invited Session - RTL Validation and Debug

#### Automated RTL Debugging with Functional and Hierarchical Abstraction

Sean Safarpour - Vennsa Technologies  
Andreas Veneris - University of Toronto, Canada

#### STAR: Generating Validation Inputs by Static Analysis of RTL

Shobha Vasudevan - University of Illinois at Urbana-Champaign

11:05am - 11:20am **Break**

11:20am - 12:30pm

### Session 3: Formal Methods for Verification

#### Learning from Constraints for Formal Property Checking

In-Ho Moon and Kevin Harer - Synopsys, Inc.

#### Exploiting Incrementality in SAT-based Search for Multiple Equivalence-Preserving Transformations in Combinational Circuits

Gianpiero Cabodi, Leandro Dipietro, Marco Murciano and Sergio Nocco - Politecnico di Torino, Italy

#### PowerRanger: Assessing Circuit Vulnerability to Power Attacks Using SAT-Based Static Analysis (Short Paper)

Jeff Hao and Valeria Bertacco - University of Michigan at Ann Arbor, USA

12:30pm - 2:00pm **Lunch**

2:00pm - 3:30pm

### Session 4: Panel - SystemC Why: To Design or to Verify?

#### Moderator and Organizer:

Sandeep Shukla - Virginia Tech, USA

#### Panelists:

John Sanguinetti - Forte Design Systems  
Brian Bailey - Industry Verification Guru  
Andres Takach - Mentor Graphics  
Chad Spackmana - Cebatech  
Ajit Dingankar - Intel  
Hiren Patel - University of Waterloo, Canada

3:30pm - 4:00pm **Break**

4:00pm - 5:40pm

### Session 5: Special Session - Innovative Industrial Practices

#### Design for Verification in System-level to RTL Design Flows

Anmol Mathur - Calypto Design Systems

#### Solving the Verification Complexity Puzzle: Predictable Verification is not an Oxymoron

Shankar Hemmady - Synopsys, Inc.

#### Current Trends in Low Power Verification for Home Network Computing

Kiran Ramineni - Marvell

#### Applying Transaction-Level Modeling on Different Abstraction Levels

Rainer Findenig - FH Hagenberg, Austria  
Volkan Esen and Wolfgang Ecker - Infineon Technologies AG, Germany  
Robert Schwencker and Michael Velten - Infineon Technologies AG, Germany

7:00pm - 10:00pm

### Banquet Dinner and Keynote Address

#### Keynote Speaker:

Sunil R. Shenoy - Vice President, Digital Enterprise Group and General Manager, Enterprise Microprocessor Group - Intel Corporation

## November 06, 2009

7:00am - 12:30pm **Registration**

7:00am - 8:00am **Breakfast**

8:00am - 9:30am

### Session 6: Test and Debug

#### Fault Table Generation using Graphics Processing Units

Kanupriya Gulati and Sunil Khatri - Texas A&M University, USA

#### Diagnostic Test Generation for Silicon Diagnosis with An Incremental Learning Framework based on Search State Compatibility

Maheshwar Chandrasekar and Michael Hsiao - Virginia Tech, USA

#### TG-PRO: A New Model for SAT-Based ATPG (Short Paper)

Huan Chen and Joao Marques-Silva - University College Dublin, Ireland

#### Localizing Transient Faults Using Dynamic Bayesian Networks (Short Paper)

Susmit Jha, Wenchao Li and Sanjit A. Seshia - University of California, Berkeley, USA

9:30am - 9:45am **Break**

9:45am - 11:00am

## Session 7: Invited Session - High-Level Modeling and Validation

### A Instrumented Observability Coverage Method for System Validation

Peter Lisherness and Kwang-Ting (Tim) Cheng - University of California, Santa Barbara, USA

### A Symbolic Execution Framework for Algorithm-Level Modelling

Ziyad Hanna - Jasper Design Automation  
Tom Melham - University of Oxford, United Kingdom

### Dynamic Verification of Multicore Communication Applications

Subodh Sharma and Ganesh Gopalakrishnan - University of Utah  
Eric Mercer - Brigham Young University

11:00am - 11:15am **Break**

11:15am - 12:30pm

## Session 8: System Validation Approaches

### Airwolf-TG: A Test Generator for Assertion-Based Dynamic Verification

Jason Tong, Marc Boule and Zeljko Zilic - McGill University, Canada

### A Versatile Scheme for the Validation, Testing and Debugging of High Speed Serial Interfaces

Yongquan Fan and Zeljko Zilic - McGill University, Canada

### Experience with Widening based Equivalence Checking in Realistic Multimedia Systems

Sven Verdoolaege - Katholieke Universiteit Leuven, Belgium  
Martin Palkovic - IMEC, Belgium  
Maurice Bruynooghe and Gerda Janssens - Katholieke Universiteit Leuven, Belgium  
Francky Catthoor - IMEC vzw, Belgium

12:30pm - 2:00pm **Lunch**

2:00pm - 3:15pm

## Session 9: Improved Verification Techniques

### A Coordinated Reachability Analysis Method for Modular Verification of Asynchronous Designs

Hao Zheng - University of South Florida, USA

### Modular Arithmetic Decision Procedure with Auto-correction Mechanism

Bijan Alizadeh and Masahiro Fujita - University of Tokyo, Japan

### Activity-based Refinement for Abstraction-guided Simulation

Debapriya Chatterjee and Valeria Bertacco - University of Michigan, USA

3:15pm - 3:30pm **Break**

3:30pm - 5:10pm

## Session 10: Invited Session - Post-Silicon Validation and Debug

### IFRA: Post-Silicon Bug Localization in Processors

Sung-Boem Park and Subhasish Mitra - Stanford University, USA

### RTL DFT Techniques to Enhance Defect Coverage for Functional Test Sequences

Hongxia Fang and Krishnendu Chakrabarty - Duke University, USA  
Hideo Fujiwara - Nara Institute of Science and Technology, Japan

### Hardware Trojan: Threats and Emerging Solutions

Rajat Subhra Chakraborty, Seetharam Narasimhan and Swarup Bhunia - Case Western Reserve University, USA

### Deign-for-Debug for Post-Silicon Validation: Can High-Level Descriptions Help?

Nicola Nicolici and Ho Fai Ko - McMaster University, Canada

# HLDVT '09

## Organizing Committee:

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**Program Chair:** Prabhat Mishra - University of Florida

**Past Chair:** Prab Varma - Blue Pearl Software

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IEEE



# Grand Hyatt San Francisco

## Directions

From San Francisco Int'l Airport (14 Miles):

Take 101 North toward the San Francisco and Bay Bridge. Exit 280 North toward "Port of SF/280 North". Stay in left lane and 280 becomes King Street. At second light, turn left onto Third St and go eight blocks to Market St. Cross over Market St. (which becomes Kearny St.) and continue two blocks. Turn left on Sutter St. Go two blocks to Stockton and Hotel is located on the left corner.

From Oakland Airport (20 Miles):

Take the Fremont St. exit (on right). Proceed 1/2-block on Fremont St. Turn left onto Howard St. Turn right onto 3rd St. Cross Market St. (street name changes to Kearny). Take Kearny two blocks to Sutter St. and turn left. Take Sutter St. to Stockton St. and turn left.

From San Jose International Airport (46 Miles)

Take 101 North toward San Francisco for approximately 43 miles. Take I-80 East toward Bay Bridge/Oakland, and then exit at Fourth Street toward Embarcadero. Make a slight left onto Bryant Street, then a left onto Third Street. Third Street will become Kearny Street. Take Kearny two blocks to Sutter St. and turn left. Take Sutter St. to Stockton St. and turn left.

## HLDVT'09 Workshop Registration Form – register online [www.hldvt.com/09/](http://www.hldvt.com/09/)

Mail or fax this form to:

**HLDVT'09**

**1721 Boxelder St., Ste. 107**

**Louisville, CO 80027 USA • Tel 303-530-4562 • Fax 303-530-4334**

**email: [register@mpassociates.com](mailto:register@mpassociates.com)**

First Name \_\_\_\_\_ Last Name \_\_\_\_\_ Company \_\_\_\_\_

Mail Stop \_\_\_\_\_ Street Address \_\_\_\_\_ City \_\_\_\_\_ State \_\_\_\_\_ Zip \_\_\_\_\_

Country \_\_\_\_\_ Phone \_\_\_\_\_ Fax \_\_\_\_\_

Email \_\_\_\_\_ IEEE Member# \_\_\_\_\_ Student # \_\_\_\_\_

Dietary Requirements \_\_\_\_\_ Vegetarian

## Advance Registration (Postmarked by October 7, 2009)

	IEEE Member	Non-member	Student Member	Student Non-member
Pre-Registration	\$465	\$585	\$295	\$350
After Oct.7	\$575	\$720	\$370	\$420

Guest Banquet Dinner @ \$100 \_\_\_\_\_ **TOTAL FEES** \_\_\_\_\_

Send full payment in U.S. dollars with this form. Use a **check drawn on a US bank or a major credit card**. For payments from non-US banks the attendee will be charged a collection fee of \$30.00. Purchase orders are not accepted.

Make checks payable to **IEEE HLDVT'09**. Use your credit card if registering by fax.

Check  Visa  Mastercard  American Express  Card # \_\_\_\_\_ Exp. date \_\_\_\_\_

Name (as it appears on card) \_\_\_\_\_ Signature \_\_\_\_\_ Sec. code \_\_\_\_\_

I agree to pay the total amount according to the card issuer agreement.

**Refunds:** Requests for refunds received before October 7, 2009, will be subject to a \$50 processing fee. No refunds will be made for cancellations received after October 7, 2009, and all registration fees will be forfeited. Faxed or mailed registrations will be accepted through October 23, 2009. Online registration will be accepted through October 30, 2009.

## HLDVT'09 Hotel Registration Form

Register before **Tuesday, October 21, 2009 at 5:00pm PST**, for the HLDVT'09 discounted room rate. Hotel space is limited. Please register before October 21, 2009, to avoid disappointment.

Mail or fax this form to:

Grand Hyatt San Francisco

345 Stockton St.

San Francisco, CA 94109 USA

Tel: +1 415-398-1234 Fax: +1 415-391-1780

Hotel Registration online: HLDVT Group Code: G-IKEE  
<http://www.grandsanfrancisco.hyatt.com/>

First Name \_\_\_\_\_ Last Name \_\_\_\_\_ Company \_\_\_\_\_

Mail Stop \_\_\_\_\_ Street Address \_\_\_\_\_ City \_\_\_\_\_ State \_\_\_\_\_ Zip \_\_\_\_\_

Country \_\_\_\_\_ Phone \_\_\_\_\_ Fax \_\_\_\_\_

**Hotel rates - Single/Double \$140.00**

**Extra person: \$25.00**

Arrival Date \_\_\_\_\_ Departure Date \_\_\_\_\_

Cancellation Policy: Should guest cancel a reservation, the Hotel shall refund deposits if notice is received prior to 6:00pm on the arrival date.

Your reservation can be guaranteed by credit card. Your credit card will be billed for first night's deposit. Sales/room tax is fifteen and a half (15.5%) percent. A California tourism assessment fee of thirteen cents (\$0.13) will apply per room, per night.

Check  Visa  Mastercard  American Express  Card # \_\_\_\_\_ Exp. date \_\_\_\_\_

Name (as it appears on card) \_\_\_\_\_ Signature \_\_\_\_\_ Sec. code \_\_\_\_\_

I agree to pay the total amount according to the card issuer agreement.