

HLDVT 2010 Final Program

Place: Anaheim Convention Center, Room 304 A

June 11, 2010

7:00am - 7:50am, Room 304A: Breakfast

8:00am - 8:05am Welcome Address

Session 1: Having Too Many and Too Few Clocks

8:05am - 9:10am

Session Chair: Namrata Shekar, Synopsys, USA

Obtaining Consistent Global State Dumps to Debug Systems on Chip with Multiple Clocks (**Invited**)

Bart Vermeulen and Kees Goossens – NXP, Netherlands

System Level Simulation Guided Approach to Improve the Efficacy of Clock-gating (**SP**)

Sumit Ahuja, Wei Zhang and Sandeep Shukla - Virginia Tech

State Space Reductions for Scalable Verification of Asynchronous Designs (**SP**)

Haiqiong Yao, Hao (Hank) Zheng – Univ. Southern Florida and Chris Myers – Univ. of Utah

Break 9:10am - 9:20am

Session 2: (Special) - Firmware Validation

9:20am - 10:50pm

Session Chair: Priyadarsan Patra, Intel

Firmware: Is this software validation? (**SP**)

Ariel Cymbarknoh¹ and Christos Kolonis, Client Components Group, Jerusalem, Israel¹ and Folsom CA, USA

Neither Seen Nor Heard: An Alternative View of the State of Firmware

Robert P Hale and Vincent Zimmer, Software Solutions Group, Intel® Corp.

Runtime Xeon Server Firmware Validation Challenge

Mohan J. Kumar, Server Development, Intel Corp.

Validating the Security of Firmware on x86-based Platforms: Experiences and Challenges (**SP**)

Salvador Mandujano, Intel Security Center of Excellence

Break: 10:50am - 11:05am

Session 3: (Tutorial) Concise, precise and powerful: IEEE 1800-2009 SystemVerilog Assertions

11:05pm - 12:00pm

Session Chair: Marc Boulé, ETS, Canada

Presenter: Surrendra Dudani- Synopsys, USA

Lunch, Room 304B: 12:00pm - 1:30pm

Entrée: Creole Swordfish or Butternut Squash Ravioli

Notes:

1. SP – Short Paper (15 minutes talk + 5 minutes Q/A)
2. Presentation time for all other papers is 25 minutes (20 minutes talk + 5 minutes Q/A)

Session 4: Other High Level: Arithmetic and Tools

1:30 - 2:30pm Session Chair: Shireesh Verma, Conexant

Analysis of Range and Precision for Fixed-Point Linear Arithmetic Circuits with Feedbacks (**SP**)

Omid Sarbishei, Yu Pang and Katarzyna Radecka – McGill Univ., Montreal, Canada

Retiming Arithmetic Datapaths using Timed Taylor Expansion Diagrams (**SP**)

Daniel Gomez-Prado, Maciej Ciesielski, Dusung Kim – U.Mas and Emmanuel Boutillon, LabSTICC, France

HIFSuite: Tools for HDL Code Conversion and Manipulation (**SP**)

Giuseppe Di Guglielmo, Franco Fummi, Graziano Pravadelli and Nicola Bombieri – Univ. Verona, Italy

Session 5: Advances in Formal Methods

2:40pm - 3:45pm

Session Chair: Sivaram Gopalakrishnan, Synopsys, USA

Quick Formal Modeling of Communication Fabrics to Enable Verification

Satrajit Chatterjee, Michael Kishinevsky, Umit Ogras - Intel

An Improvement in Decomposed Reachability Analysis for Symbolic Model Checking (**SP**)

Nicholas Donataccio and Hao Zheng - Univ. Southern Florida

Semi-Formal Functional Verification by EFSM Traversing via NuSMV (**SP**)

Giuseppe Di Guglielmo, Franco Fummi, Graziano Pravadelli, Stefano Soffia – Univ. Verona and Marco Roveri- FBK, Italy

Session 6: (Special) Accelerators and Emulators

4:05pm - 5:25pm Session Chair: Jai Kumar, Intel

Towards Emulation-based System-level Verification Environments – an Industrial Approach (**SP**)

Wisam Kadry - IBM Research, Israel

Compiling and Executing Verilog on Time-multiplexed FPGAs and Massively Parallel Processor Arrays (**SP**)

Guy Lemieux - Univ. of British Columbia, Canada

Levering the Transaction Nature of OVM Testbenches to Boost Hardware Emulation Performance (**SP**)

Jim Kenney – Mentor Graphics, USA

Integrated Flows for Emulation-based Verification (**SP**)

Ashutosh Varma – Cadence Design Systems, USA

Panel: Clock Domain Verification Challenges

5:30pm – 6:50 p.m.

Moderator: Prab Varma, Blue Pearl Software, USA

Iredamola Olopade -Intel, Pranav Ashar - Real Intent, Harry Foster –Mentor, Shaker Sarwary - Atrenta

Dinner, Catal Restaurant: 7:30pm - 10:30pm

Entrée: Grilled flank steak with Fontina cheese mashed potatoes or Orchiette pasta with fresh market peas.

(Directions and map are in the next page)

June 12, 2010

7:00am - 12:30pm Registration
7:00am - 8:00am, Room 304A: Breakfast

Session 7: Coverage and Constraints

8:00am - 9:20am Session Chair: Vijay Durairaj, Synopsys
Towards Analyzing Functional Coverage in SystemC TLM Property Checking (SP)
Hoang M. Le, Daniel Grosse and Rolf Drechsler – Univ. Bremen
Coverage Metrics for Verification of Concurrent SystemC Designs Using Mutation Testing (SP)
Alper Sen and Magdy Abadir- Freescale, USA

Static Analysis of Deadends in SVA Constraints (SP)
Ashvin Dsouza - Synopsys, USA

A Case Study of Time-Multiplexed Assertion Checking for Post-Silicon Debugging (SP)
Ming Gao and KT Cheng – Univ. California, Santa Barbara, USA

Break 9:20am - 9:35am

Session 8: (Special) - Transaction-Level Modeling

9:35am - 11:00am Session Chair: Heon-mo Koo, Intel
TLM-based System-level Validation using VMM for HW/SW co-simulation and co-verification (SP)
Nasib Nasser - Synopsys, USA

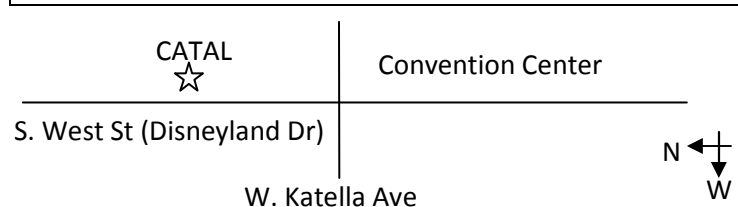
Fast and Accurate UML State Chart Modeling using TLM+ Control Flow Abstraction
Wolfgang Ecker - Infineon, Germany, Rainer Findenig - Upper Austrian Univ. of Applied Sciences, Austria, Thomas Leitner - DICE, Austria, Michael Velten - Infineon, Germany

Automatic Generation of Host-Compiled Timed TLMs for High Level Design (SP)
Samar Abdi - Concordia Univ.

Automatic Synthesis of OSCI TLM-2.0 Models into RTL Bus-based IPs (SP)
Nicola Bombieri, Franco Fummi and Valerio Guarnieri – Univ. of Verona

Break 11:00am - 11:15am

Dinner Directions: Catal Restaurant is at 1580 Disneyland Dr, Anaheim 92802. This street is the first one to the west from Convention Center reachable by either Katella or W. Convention Way going towards West. The restaurant is 500m north of W. Katella Ave. on the right side of the S. West St (Disneyland Dr).



Session 9: Systems and Modeling

11:15am - 12:30pm
Session Chair: Shankar Hemmady, Synopsys, Inc., USA
Automated Synthesis of EDACs for FLASH Memories with Adaptive Correction Capability (SP)
Michele Fabiano, Andrea Miele, Roberto Piazza and Paolo Prinetto - Politecnico di Torino, Italy, Maurizio Caramia - Thales Alenia Space Italia, Italy

Utility of Transaction-Level Hardware Models in Refinement Checking (SP)
Yogesh Mahajan and Sharad Malik – Princeton Univ.

An Ontology and Constraint Based Approach to Cache Preloading
Rajiv Bhatia, Eyal Bin, Eitan Marcus and Gil Shurek - IBM

Lunch, Room 304B: 12:30pm - 2:00pm

Entrée: Grilled Ancho Spiced Chicken or Stuffed Eggplant Roulade

Session 10: (Special) Verification Challenges at ESL

2:00pm - 3:15pm
Session Chair: Stephan Bourduas, Intel, USA

ESL Flows are Enabled by High-Level Synthesis with Universality, Rishiyur Nikhil - Bluespec, USA

Using Code Coverage with SystemC and High-level Synthesis
John Sanguinetti – Forte Design Systems, Eugene Zhang - Jeda

ESL Design and Multi-Core Validation using the System-on-Chip Environment
Weiwei Chen, Xu Han and Rainer Doemer – UC, Irvine

Break 3:15pm - 3:30pm

Session 11: (Special) – HW-dependent Software Validation

3:30 - 5:10pm Session Chair: Henry H. Y. Chan, IBM
Model Reduction Techniques for the Formal Verification of Hardware-dependent Software
Thomas Steininger, Michael Velten, Volkan Esen, Wolfgang Ecker, Rainer Findenig - Infineon Technologies

Integrating Architectural Constraints in Application Software by Using Model Transformations in BIP
A. Basu, S. Bensalem, P. Bourgos, M. Bozga and Joseph Sifakis - Verimag

Verification of Real-Time Properties for Hardware-dependant Software
Wolfgang Mueller, Marcio Olivera, Henning Zabel - Univ. of Paderborn/C-LAB

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